RELIABILITY ANALYSIS OF LOW LEAKAGE FULLY SELECTED 11t SRAM

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Abstract:

In order to perform bit interleaving, this study proposes two architectures of 11T SRAM cells that are totally half select-free. The proposed 11T-1 and 11T-2 cells use power-cutoff and write '0'/ '1' only strategies to effectively reduce Read disturb and Write half-select disturb, while simultaneously improving Write-ability. At VDD=0.9V, the 11T-1 and 11T-2 cells outperform the 6T cell in both read and write yield by about 2 times. Mean Write-margin (WM) for the proposed 11T-1 cell is 13.6% greater than that of the present 11T cell. Neither of the suggested cells suffers from the write half-select floating node problem that plagued prior power cutoff cells. Low-voltage functioning with no auxiliary circuits is confirmed by Monte-Carlo simulation. We also provide a comparative examination of how the predictability of 32nm high-k metal gate CMOS technology affects the dependability of Bias Temperature Instability (BTI) in SRAM performance. The Read Static Noise Margin (RSNM) decreases for all cells when subjected to static stress. Ripple Carry Adder (RCA), Kogge Stone Adder (KSA), Brunt Kung Adder (BKA), Cadence, Adder-based Multiplier, Gate count, number of transistors, Power, and Delay are some examples of relevant keywords.

1.INTRODUCTION

Power dissipation has become a major design restriction due to the increasing use of low-power devices such as wireless sensor networks, implanted biomedical devices, and other battery-operated portable gadgets. Power consumption is mostly attributable to static random-access memory (SRAM), which already makes up a sizeable fraction of and is expected to account for an even larger fraction of SoCs in the future [1]. Furthermore, the leakage becomes a major concern with the development of ultra-scaled technology. As Vth and gate oxide thickness decrease, leakage increases exponentially, leading to a corresponding rise in power consumption [2]. As a result, achieving a power efficient architecture requires reducing the amount of energy used by SRAM. Because active power decreases quadratically with supply voltage and leakage power decreases exponentially with supply voltage [3], lowering the supply voltage is a simple technique to improve power efficiency. However, manufacturing variation drastically reduces SRAM cell performance at lower supply voltages [4]. As a result, standard 6T SRAM has a far higher chance of failing during Read/Write operations owing to the difficulties of keeping the device strength ratio in the subthreshold region stable [5]. To prevent Read failure, numerous different layouts of SRAM cells have been suggested [6]–[13]. Decoupling the read and write paths increases the read static noise margin (RSNM) of these cells, but they still have a low write margin (WM) in the subthreshold region. To further improve the write margin of the SRAM cell, other write-assist strategies have been published in the literature [14–20]. Common write-assist approaches that increase write-ability by bolstering the driving capabilities of the write access transistor include word line (WL) boosting [14], [15] and negative bit line (NBL) [16]. However, there are space and energy costs associated with using these methods. Another helpful technique for improving write-ability is to reduce the power of the cross-coupled inverter pair. Among them include turning off the power [17, 18], increasing the voltage [19, 20], and floating the cell VSS [11, 20]. Since the effective distance between transistors has shrunk in ultra-scaled technology, Multi-bit soft error/upset (MCU) has become a danger to the reliability of SRAMs [21]. An effective method of handling this kind of mistake is the Bit interleaving (BI) architectural strategy. However, this method works for cells that never display any signs of half-select (HS) action. Using cross-point cell selection, where a write route comprises of two access transistors controlled by separate row and column-based signals [10], is the simplest way to achieve HS-free operation. However, write-ability is greatly degraded by stacked transistors in the write-access channel, necessitating WL boosting for both the row-based and column-based Write WL at the price of dynamic power. The two suggested BI cells, 11T [17] and 12T [18], both make use of cross-point chosen series-connected access transistors to once again get rid of HS disturb. yet, the Write-ability of these cells is enhanced by Power Cutoff Write-assist, and they do not need word line boosting; yet, the quality of the data stored in the nodes Q and QB in the column

write degrades at the floating-1 level. cell types with HS prefix.

To ensure the integrity of the data stored in the column write half-select (CHS) cells, they call for an additional Pulse Width-Controller to be included in the column circuitry. However, the power cut-off employed during the write operation once again causes floating of data at storage nodes Q in row half select (RHS) cells, despite the fact that a BI power gated 9T cell [22] has been developed to overcome the HS problem. To address this problem, we propose two novel 11T cells that use a BI design to boost MCU immunity and eliminate the need for write-back or any other kind of assistance. Increasing writability is accomplished in two different ways: in 11T1, the supply is cut off and a '0' is written, while in 11T-2, the ground is cut off and a '1' is written. In contrast to the current 11T [17], power outages in proposed cells do not cause data storage nodes in any HS cell to float. Designing SRAMs with high reliability in deep submicron technologies is difficult. Reliability issues arise when scaling below the 32nm node, since devices gradually degrade with use and time. One of the most serious problems with device dependability brought on by rapid scaling is bias temperature instability (BTI). Once the primary reliability issue in PMOS devices, negative bias temperature instability (NBTI) is now the primary reliability issue in NMOS devices due to the introduction of high-k metal gates and their reliance on charge trapping [23]. Both NBTI and PBTI worsen circuit performance because they raise the transistor's threshold as stress time progresses. Therefore, it is essential to investigate the effect of NBTI and PBTI on various SRAM performance indicators. This paper also includes an analysis of the proposed cells' BTI reliability to determine how transistor aging affects performance parameters including Read SNM, Write-Margin, Read/Write latency, Read/Write power, and leakage power.

2.LITERATURE SURVEY

10T SRAM Low Switching Power and Ultralow RBL Leakage with Half-VDD Recharge and Row-Wise Dynamically Powered Read Port

For low power operation and leakage reduction, this study introduces a novel 10T static random access memory cell with a single ended decoupled read-bit line (RBL) and a 4T read port. The RBL is first charged to 50% of the cell's supply voltage and then discharged and charged again in accordance with the information bit. During the read operation, the RBL is connected to the virtual power rails through a transmission gate and an inverter operated by the supplementary data node (QB). For a read-1, RBL rises toward the VDD level, whereas for a read-0, it falls. During the write and hold modes, virtual power rails are recharged to the same RBL level, and only during the read operation are they linked to the real supply levels. By dynamically regulating the virtual rails, RBL leakage may be drastically cut down.A commercial 65 nm technology yields a 10T cell that is 2.47 times smaller than a 6T cell with = 2, has a 2.3-times larger read static noise margin, and cuts read power dissipation by 50 percent compared to a 6T cell. When compared to the 6T BL leakage, the RBL leakage value is lowered by more than three orders of magnitude, and the ION/IOFF ratio is vastly improved. Overall, 6T and 10T leakage characteristics are comparable, and comparable performance is attained.

Low Air Loss BTI Reliability Analysis for Fully Half-Select-Free SRAM Cells

In order to achieve bit-interleaving, this work proposes two distinct topologies of 11T SRAM cells that are totally half-select-free. The proposed 11T-1 and 11T-2 cells use power-cutoff and write '0'/ '1' only strategies to effectively reduce Read disturb and Write half-select disturb, while simultaneously improving Write-ability. At VDD=0.9V, the 11T-1 and 11T-2 cells outperform the 6T cell in both read and write yield by about 2 times. Mean Write-margin (WM) for the proposed 11T-1 cell is 13.6% greater than that of the present 11T cell. Neither of the suggested cells suffers from the write half-select floating node problem that plagued prior power cutoff cells. Low-voltage functioning with no auxiliary circuits is confirmed by Monte-Carlo simulation. We also provide a comparative examination of how the predictability of 32nm high-k metal gate CMOS technology affects the dependability of Bias Temperature Instability (BTI) in SRAM performance. The Read Static Noise Margin (RSNM) decreases for all cells when subjected to static stress.

Process-variation-tolerant ultra-low voltage Construction of a Schmitt-Trigger SRAM

We investigate differential-sensing Schmitt-Trigger (ST) static RAM (SRAM) bit cells for ultralow-voltage use. The ST-based SRAM bit cells solve the problem of a standard 6T bit cell's read and write operations being at odds with one another. The ST operation improves both read- and write-stability over the more common 6T bit cell. The suggested ST bit cells include an in-built feedback mechanism that

allows for process variation tolerance, a feature essential for the next generation of nanoscale technology nodes. The ST-2-bit cell has been shown to be operable at lower supply voltages in a comprehensive evaluation of other bit cells under iso-area condition. Ten test-chips built using 130-nm CMOS technology yielded measurements indicating that the proposed ST-2-bit cell provides a 1.6-fold improvement in read static noise margin, a 2-fold improvement in write-trip-point, and a 120-mV reduction in read min compared to the iso-area 6T bit cell.

9T SRAM circuit with strong, low-leakage SLEEP mode that is resistant to variations

Due to the deterioration of data stability, weakening of write ability, rise in leakage power consumption, and aggravation of process parameter changes that come with scaling CMOS technology, the design of static random-access memory (SRAM) circuits is difficult. In this research, we present a circuit for a low-leakage SLEEP mode with data retention using a nine-transistor (9T) asymmetric ground-gated metal-oxide semiconductor random-access memory (MTCMOS). Under die-to-die process parameter variations in a 65nm CMOS technology, the asymmetrical 9T SRAM cells outperform conventional 6T and 8T SRAM cells by up to 2.52x and 21.84%, respectively, in terms of static noise margin and write voltage margin. Additionally, under within-die process parameter changes, the new 9T SRAM cells improve the mean values of static noise margin and write voltage margin by up to 2.58x and 21.78%, respectively, as compared to the traditional 6T and 8T SRAM cells.

3.PROPOSED SYSTEM

A.Proposed 11T-1 Cell

The 11T-1 SRAM cell's conceptual diagram may be seen in Fig. 1. The power cut-off with floating-avoidance assist (PCFA) is an integral part of the cell's cross-coupled inverter. To enhance write-ability, the PCFA network's MP1 and MP3 transistors internally reduce the supply voltage, which shorts off the pull-up circuit and allows for a contention-free discharge of the storage node. In contrast, CHS cells with transistor MP2, driven by row-based WL, never experience the floating-1 problem. The MAL and MAR write access transistors are regulated by the WLA and WLB signals, which are column based. The varying states of the control signals during the various modes of operation of the proposed cells are shown in Table. WLA and WL signals are turned on during a Write '0' operation, whereas WLB and VVSS are turned off. By turning off power to the left inverter, node Q may be quickly drained through transistors MAL and MR2. As before, writing '1' activates the WL and WLB while deactivating the WLA. Right inverter's power has been switched off;therefore, charge may be quickly removed from node QB through MAR and MR2, leading to the '1' being recorded at node Q. Turning on the WL signal while maintaining a '0' value for WLA and WLB completes the read process. When performing a read operation, the RBL is charged in advance. Based on the information at QB, the discharge route for RBL via transistors MR1 and MR2 will be enabled. By turning off the WLA and WLB signals during a read access, the data storage nodes (Q and QB) are completely cut off from the rest of the network. Therefore, even for subthreshold operation, the ‘read upset' is of little issue. All control signals are cut off while in Hold Mode, isolating the cross-coupled inverters and eliminating the need for a floating node. Thus, in the hold mode, the cell is as stable as a 6T cell. Maintaining a strong VVSS signal during standby mode greatly minimizes static power usage. 11T-2 Cell Proposal, Part B A conceptual drawing of the 11T-2 SRAM cell is shown in Fig. 2. The same three MNs (MN1, MN2, and MN3) make up its Ground-cutoff with floating avoidance aid (GCFA) network. The GCFA's write-ability is enhanced by the internal ground cut-off provided by transistors MN1 and MN3 and the contention-free charging of the high-going node they enable. While enhancing the storage node's write-ability via contention-free discharge. In contrast, CHS cells with transistor MP2, driven by row-based WL, never experience the floating-1 problem. The MAL and MAR write access transistors are regulated by the WLA and WLB signals, which are column based. The multiple modes' control signal states are shown in table I.

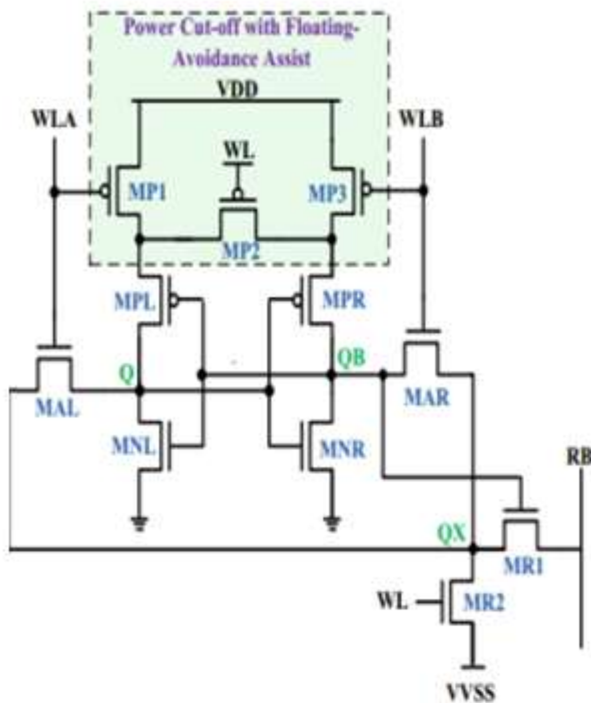


Fig 1 proposed ill 1cell schematic

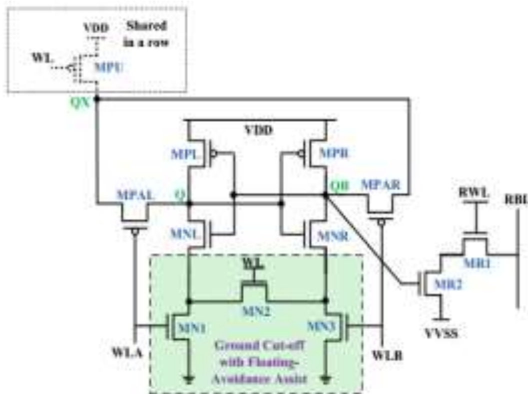


Fig. 2. Proposed 11T-2 cell schematics.

shows how the planned cells work in operation. WLA and WL signals are turned on during a Write '0' operation, whereas WLB and VVSS are turned off. By turning off power to the left inverter, node Q may be quickly drained through transistors MAL and MR2. In a similar vein,

If you enter '1', WL and WLB will be turned on but WLA will be turned off. Having severed power to the right inverter, node QB is now simply discharged through MAR and MR2, leading to the '1' being recorded at node Q. Turning on the WL signal while maintaining a '0' value for WLA and WLB completes the read process. When performing a read operation, the RBL is charged in advance. Where the waste is going

TABLE I
CONTROL SIGNALS DURING VARIOUS MODES OF OPERATION FOR THE PROPOSED 11T-1/11T-2 CELL

Control Signal	Operation			
	Hold	Read	Write '0'	Write '1'
WLA	0/1	0/1	1	0
WLB	0/1	0/1	0	1
WL	0/1	1/0	1/0	1/0
RBL	1	Pre	0/1	1
RWL	0	1	0	0
VVSS	1	0	0/1	0/1

based on the information kept at QB, will turn on RBL through transistors MR1 and MR2. By turning off the WLA and WLB signals during a read access, the data storage nodes (Q and QB) are completely cut off from the rest of the network. Thus, the 'read disturbed' serves no use. worry even for below-threshold functioning. When the Hold Mode is activated, all control signals are cut off, isolating the cross-coupled inverters and eliminating the need for a floating node. Thus, in the hold mode, the cell is as stable as a 6T cell. By maintaining a strong VVSS signal during standby, static power consumption is drastically reduced.

B. Proposed 11T-2 Cell

A conceptual drawing of the 11T-2 SRAM cell is shown in Fig. 2. Ground-cutoff with floating avoidance assist (GCFA) is made up of MN1, MN2, and MN3 and is comparable to the core of the original cell. Transistors MN1 and MN3 are located on the inside of the GCFA. Write performance may be enhanced by isolating the ground during operations and allowing the high-performing node to charge without interference. In contrast, transistor MN2, which is row-based WL's driver, prevents '0's from floating in CHS cells. Single-ended sensing with a read buffer implemented by the MR1 and MR2 transistors is used in this cell. In order to prevent leaking during standby, VVSS signal is employed. Signals based on columns, WLA and

WLB, regulate the MPAL and MPAR write access transistors. The row-based WL signal controls the transistor MPU that is shared by many rows. While WLB and WL signals are turned off, WLA is activated during a Write '0' operation. Pulling node QB up via transistors MPAR and MPU is uncontended by pull-down transistor MNR since the right inverter is isolated from the ground line. Therefore, Q is lost to ground through MNL and MN1. Since the '1' is written in the same way, the process is symmetrical.

C. Write-Half-select

Cellular Function Any unselected cells in the selected rows or columns will be disturbed in the storage node during the write operation, and this is referred to as a "half-select disturb." For the SRAM cell to be employed in BI architecture, which addresses multibit faults, HS-free operation is required. The BI method only uses a single bit of a word at a given position, as opposed to the whole word. Therefore, it is identical to when data disturbance happens at many bits locally. single-bit errors in several words, which are readily fixed with a standard Error-correcting code (ECC). The suggested 11T cells not only fix the HS problem, but also prevent the storage nodes from experiencing the floating node state. In order to prevent write HS disturb, the prior 11T cell [17] relied on cross-point addressed write access. The CHS cell undergoing a write '1' operation is seen in Fig. 3. CHS cell MP3 players and power cutoff switches will be disabled as well. If QB is holding a '1', the voltage will drop because it will become "floating." This floating node issue will get much more serious when parameters are used.

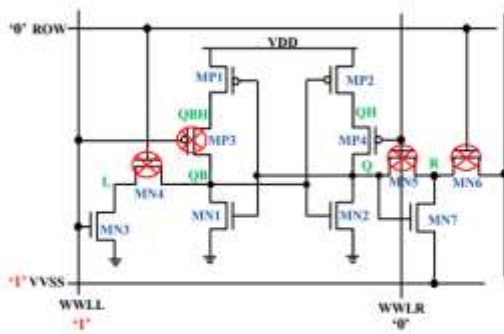
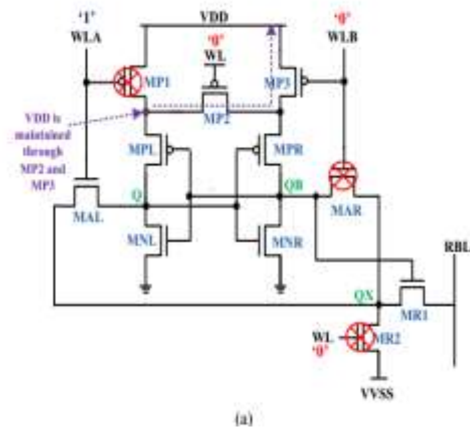
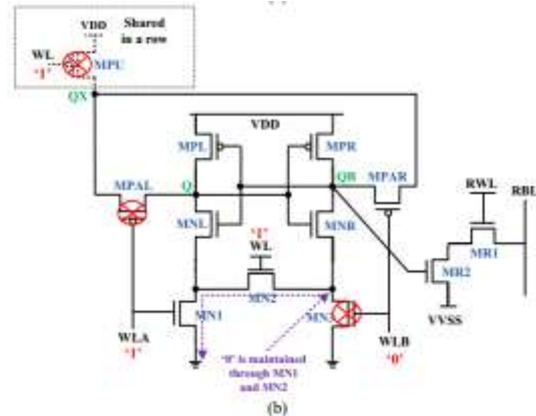


Fig. 3. Column Half-selected cell under write '1' opeartion for previous power cut-off 11T cell [17].

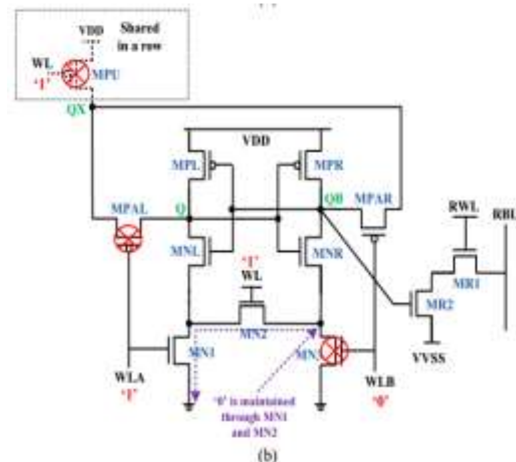


(a)



(b)

Fig. 4. Column Half-select cell under write '0' operation in (a) 11T-1 (b) 11T-2 cell.



(b)

Fig. 4. Column Half-select cell under write '0' operation in (a) 11T-1 (b) 11T-2 cell.

fluctuations in low-voltage power supplies that might cause data to be flipped. With 5,000 iterations of Monte Carlo simulation at TT, 25°C (simulation is done for 16nm CMOS predictive technology model),

Fig. 5 displays the transient waveform of CHS cells of different SRAM cells. [24]). Similarly, node Q experiences a floating-'1' scenario while performing a write '0' operation, since MP4 of the CHS cell is turned off. Due to the high voltage level of VVSS, node R is also being pushed up by MN7, therefore the fall in voltage at node Q will be considerably slower. Therefore, in this scenario, the data retention period will be considerably longer, defined as the maximum amount of time that nodes may store data before flipping. Figure 5 demonstrates that both Q=1 and Q=0 cases of floating nodes in the 11T CHS cell [17] cannot be recovered and cause data flipping. Nanoscale technologies cannot be used to accomplish rob operation of CHS cells in this cell type. For RHS cells, the proposed 11T-1 cell turns off its write access transistors, isolating the cell core from any potential disruptions. The write '0' operation of the 11T-1 cell is shown in Fig. 4(a). WLA is strong, whereas WL and WLB are weak. When WL is 0, MR2's access transistor is disabled. In the Q=1 situation, when MR1 is likewise invalid, there is no write disturb route. When Q=0, however, MR1 will be active and Q will be available to RBL without any intermediate steps. Even so, Q will remain undisturbed while RBL is likewise set to 0. Since the pullup route for the left inverter has been severed, the PMOS switch MP1 is also off. However, since WL is low, the floating avoidance assist switch, MP2, is activated, which aids in keeping Q from drifting off the pull-up path. Due to the symmetric nature of the CHS cells in the proposed 11T-1, a similar behavior is seen for the write '1' case as well. In Fig. 5, we can see that after running 5000 MC simulations, the floating Q=1 (also QB=1 under write '1' operation) in the CHS cell of 11T-1 has been fully restored, with no instances of data flipping. 3) 11T-2 cell: MPAL and MPAR are both turned off and the cell core is unaffected in the planned 11T-2 cell line, as is the case with RHS cells.

path. Figure 4(b) depicts a CHS cell undergoing an 11T-2 write '0' operation. Since MPU is activated for just the chosen rows, CHS cells are totally shielded from the path of disruption caused by writing.
WLB is '0', as illustrated in Fig. 4(b), which disables MN3 and hence the pull-down pathway. QB may float during write access if it stores a '0,' but the floating avoidance switch MN2 helps to keep it at the '0' level. During a write '1' operation, the left inverter's '0' state is kept alive through MN2 and MN3. In Fig.5, we can see that after running 5000 MC simulations, the floating QB=0 (also Q=0 during write '1' operation) in the CHS cell of 11T-2 has been fully recovered, and that no cases of data flipping have been recorded.

III. BTI ANALYSIS FRAMEWORK.

When a negative bias is supplied to the gate of a PMOS transistor, NBTI occurs, whereas a positive bias result in PBTI in an NMOS transistor. The threshold voltage of the transistor rises under these circumstances, known as stress mode. The BTI-Induced When the stress situation is switched around, such that PMOS is positively biased and NMOS is negatively biased, some of the lost quality is restored. Interface traps arise when the gate-source voltage of a PMOS transistor is negative, since this causes holes from the inversion layer to break the Si-H bond at the Si-SiO2 interface. These traps are of a positive nature, becoming apparent when the transistor's threshold voltage rises. Poly gate has very low PBTI, while high-k metal gates have elevated it to levels above those of NBTI. Recently, DC and AC NBTI (PBTI) have been described by a physics-based model consisting of uncorrelated trap generation (TG) and trapping (electron and hole) [25]. This model follows the response diffusion (R-D) paradigm for BTI under conditions of static and relaxed stress. In the same way that n has an exponent of time about equal to 0.16, as seen in equation (1).

$$\Delta V_{t\square} \cong K_{ac} \times t^{n} \cong \propto (S,f) K_{dc} \times t^{n}$$

The parameter 'n' represents the time exponent, while 'DC' is the constant that varies with technological advancements. The AC degradation factor is the activity factor (S, f), which depends on the duty cycle (S) and frequency (f) of the signal. However, it is determined that frequency has a very little impact on the Vth.

Activity factor dependency on signal duty cycle may be roughly estimated using the formula (2)[25].

$$\propto (S,f) \cong S^{1/6}$$

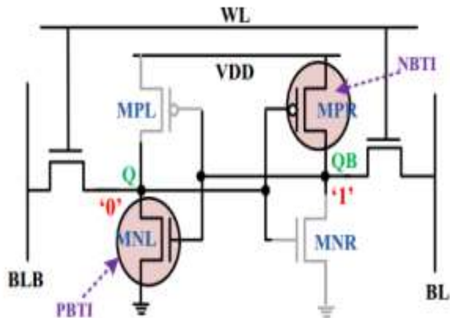


Fig. 8. 6T SRAM cell showing stress on transistors due to NBTI and PBTI.

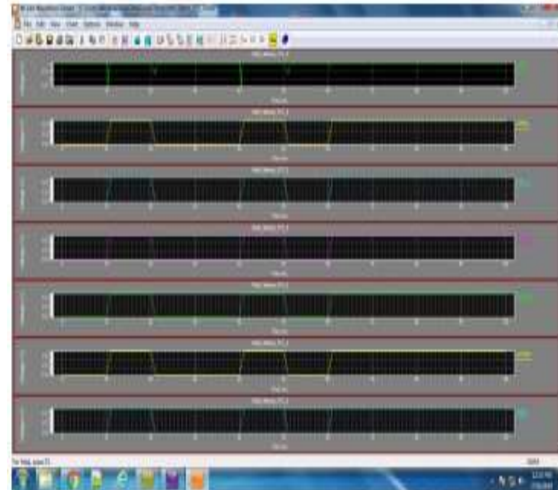
4. EXPERIMENTAL RESULTS

HALFSELECT-11T-2-DESIGN

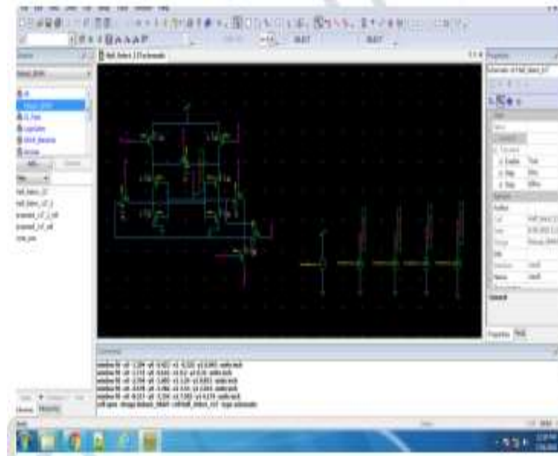
HALFSELECT-11T-2-POWER

```
Power Results
Total Power from time 0 to 1e-007
Average power consumed -> 1.179786e-004 watts
Max power 9.543581e-003 at time 1.04653e-008
Min power 1.167407e-009 at time 6.25e-010

* END NON-GRAPHICAL DATA
*

* Parsing                      0.01 seconds
* Setup                        0.02 seconds
* DC operating point           0.00 seconds
* Transient Analysis           0.03 seconds
* Overhead                     0.22 seconds
* -----------------------------------------
* Total                        0.28 seconds

* Simulation completed
```

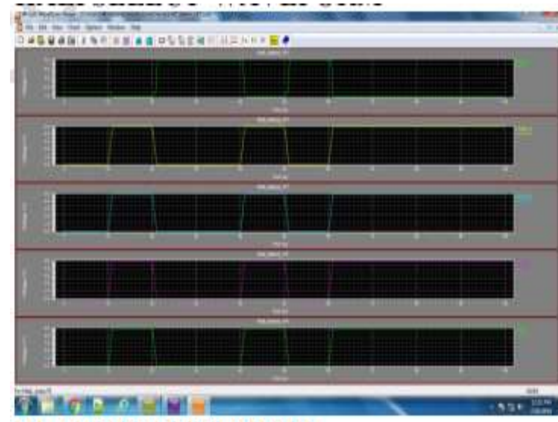
HALFSELECT-11T-2-WAVEFORM



HALFSELECT-DESIGN



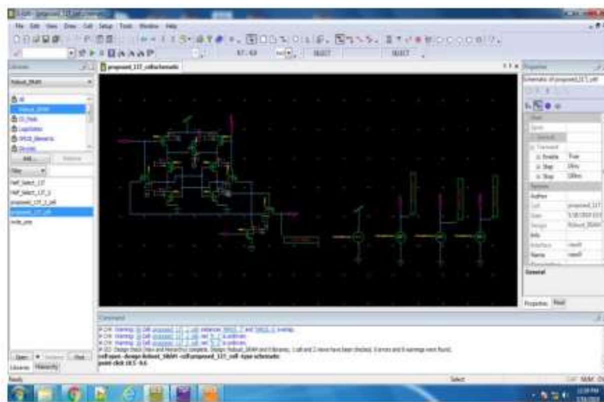
HALFSELECT-WAVEFORM



HLAFSELECTPOWER

```
Power Results
Total Power from time 0 to 1e-007
Average power consumed -> 1.927806e-003 watts
Max power 7.328286e-003 at time 2.0875e-008
Min power 3.209113e-005 at time 4e-008

* END NON-GRAPHICAL DATA
*

* Parsing                        0.01 seconds
* Setup                          0.00 seconds
* DC operating point             0.00 seconds
* Transient Analysis             0.03 seconds
* Overhead                       0.51 seconds
* -----------------------------------------
* Total                          0.56 seconds

* Simulation completed  with  2 Warnings

* End of T-Spice output file
```

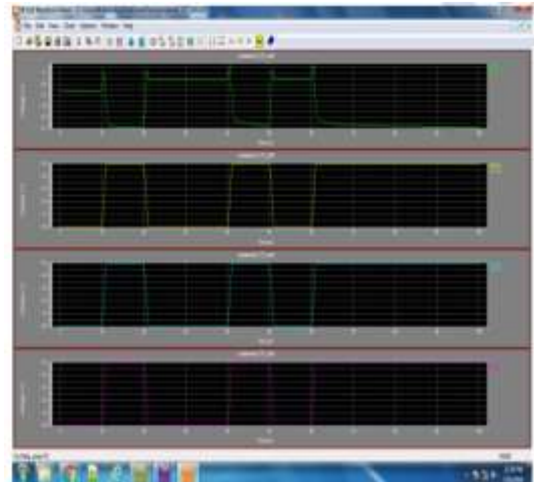
PROPOSED-11T-1-DESIGN



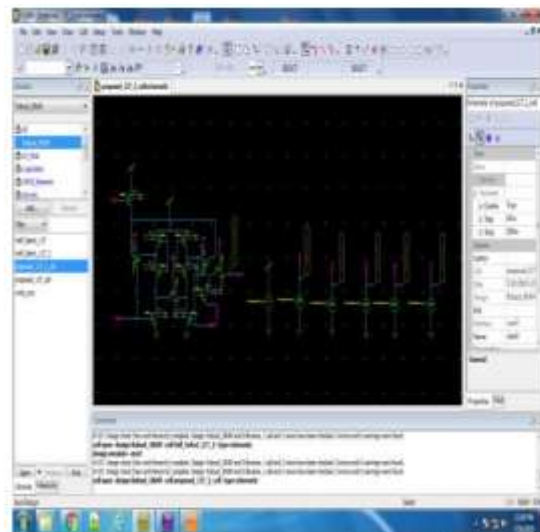
PROPOSED-11T-1-POWER

```
* BEGIN NON-GRAPHICAL DATA

Power Results
Total Power from time 0 to 1e-007
Average power consumed -> 2.915871e-003 watts
Max power 7.536684e-003 at time 5.1e-008
Min power 8.372559e-009 at time 7.36215e-008

* END NON-GRAPHICAL DATA
*

* Parsing                        0.01 seconds
* Setup                          0.01 seconds
* DC operating point             0.00 seconds
* Transient Analysis             0.01 seconds
* Overhead                       1.08 seconds
* -----------------------------------------
* Total                          1.12 seconds

* Simulation completed  with  4 Warnings

* End of T-Spice output file
```

PROPOSED-11T-1-WAVEFORM



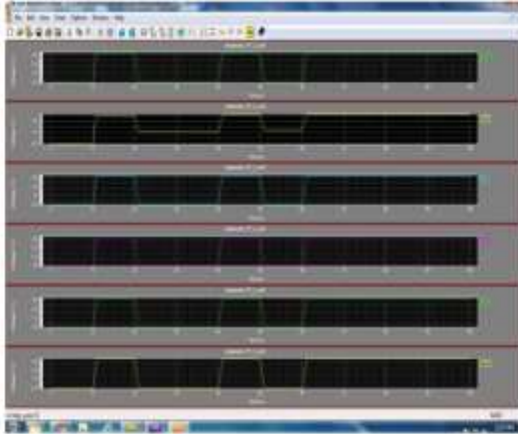
PROPOSED-11T-2-DESIGN



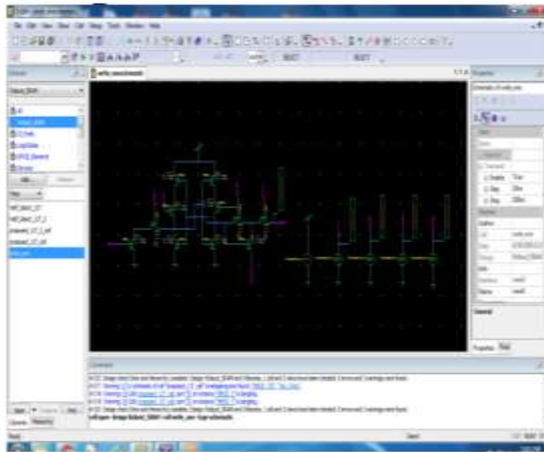
PROPOSED-11T-2-POWER

```
* BEGIN NON-GRAPHICAL DATA

Power Results
Total Power from time 0 to 1e-007
Average power consumed -> 4.655868e-003 watts
Max power 9.974520e-003 at time 1.04899e-008
Min power 2.381886e-009 at time 1e-009

* END NON-GRAPHICAL DATA
*

* Parsing                        0.03 seconds
* Setup                          0.00 seconds
* DC operating point             0.01 seconds
* Transient Analysis             0.01 seconds
* Overhead                       0.73 seconds
* -----------------------------------------
* Total                          0.79 seconds

* Simulation completed  with  3 Warnings

* End of T-Spice output file
```

PROPOSED-11T-2-WAVEFORM



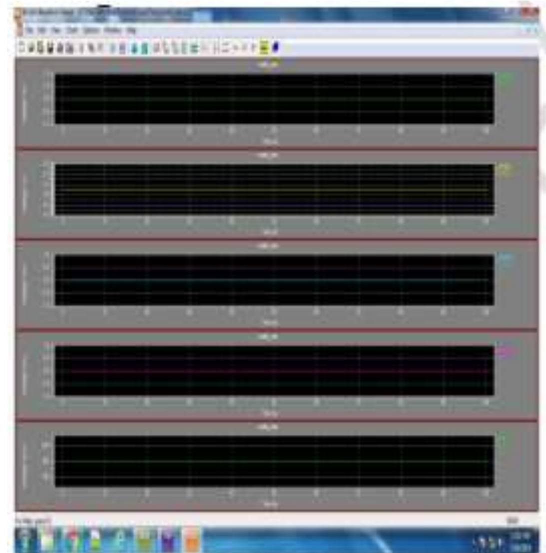
WRITE_ONE-DESIGN



WRITE_ONE-POWER

```
* BEGIN NON-GRAPHICAL DATA

Power Results
Total Power from time 0 to 1e-007
Average power consumed -> 9.162135e-003 watts
Max power 9.162135e-003 at time 0
Min power 9.162135e-003 at time 0


* END NON-GRAPHICAL DATA
*

* Parsing                          0.03 seconds
* Setup                            0.00 seconds
* DC operating point               0.00 seconds
* Transient Analysis               0.00 seconds
* Overhead                         0.81 seconds
* -----------------------------------------
* Total                            0.84 seconds

* Simulation completed  with  1 Warning

* End of T-Spice output file
```

WRITE_ONE WAVEFORM



CONCLUSION

In this study, we suggest two 11T SRAM cell topologies that are totally half-select free and resilient, making them an excellent choice for bit-interleaved designs. The suggested 11T-1 and 11T-2 cells use power-cutoff and other techniques to get rid of Read disturb, Write half-select disturb, and boost Write-ability. simple '0' and '1' only writing methods. Read and write yields for the 11T-1 and 11T-2 cells are improved above those of the 6T cell. Both suggested cells validate low-voltage functioning without requiring any extra peripheral Write- and Read-assist circuits by completely eliminating the floating node problem seen in prior power cut-off simulations. Predictive 32nm High-k metal gate CMOS technology was also used to study the effect of BTI on SRAM performance. All cells are observed to have a decreased RSNM when subjected to static stress. It was discovered, however, that 11T-1 and 11T-2 cells, thanks to BTI, exhibit enhanced RSNM.
And although the suggested cells increase write delay without affecting read delay or power over time, they also decrease write power and leakage power and enhance WM. Despite process changes and the aging impact of transistors, the suggested 11T cells have been shown to be a good option for dependable SRAM design in nanoscale technologies by means of MC and BTI analysis.

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